REMARKS

Claims 1, 3, 5-13 stand rejected under 35 USC 103(a) as being unpatentable over Everett et al. (US Patent No. 6,532,024). The Examiner reasons that the claims of the present invention are obvious over Everett et al. because Everett et al. suggests a system that can also act on interlaced format. Applicants respectfully submit that the Examiner has misunderstood the system of Everett et al. and/or the present invention and requests reconsideration of the final rejection.

The object of the system of Everett et al. is to enable an incoming interlaced video signal to be displayed on a standard non-interlaced computer monitor (see, for example, the abstract) because "the use of standard interlaced displays for simultaneous display of [video image information] severely limits the clarity and detail of the video images, rasterized waveforms, vectorscope and audio graphic display information" (see column 2, lines 27 - 31). The quoted reference at column 1, lines 42 - 48 of Everett et al. simply refers to the fact that standard interlaced displays exist which can be used for the purpose of simultaneously displaying the above-mentioned information, but this is allegedly undesirable, and Everett et al. therefore provides a system that generates a re-sized non-interlaced video image, graphic video waveform, audio phase and vector diagram based on the video input signal. This is in direct contrast to the present invention, which provides a system for generating a resized high definition interlaced video image from the original standard definition interlaced video image, such that it can be displayed in its reduced size on a high definition interlaced display without loss of reduction relative to

the reduction of the original video input signal. Thus, Everett et al. actively teaches away from the claims of the present invention.

The system of Everett et al. operates as follows. The video input signal is standard definition, interlaced signal which is first input to a video line doubler (100) to convert the YUV signals from interlaced to non-interlaced format (see column 6, lines 10 - 19). The output of the video line doubler (100) is then input to a resizing engine (102) which produces individual pixels for display on a non-interlaced video monitor.

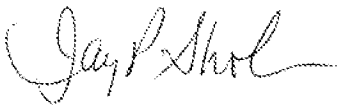
The video input signal of the claimed video signal processor is also a standard definition, interlaced signal. However, this signal is input directly to the resizing circuitry to generate a resized, standard definition interlaced picture component signal. A measurement component signal is also derived from the video input signal. In addition, a video signal generator generates a high definition, interlaced background video signal. Combining circuitry superimposes the resized picture component signal and the measurement component signal (both derived from and consequently of the same interlaced format and definition as the input signal) on the higher definition interlaced background video signal to produce a high definition, interlaced output signal. This provides a convenient way for displaying, for example, a standard definition 720 x 576 interlaced pictures on part of high definition 1920 x 1080 interlaced display without loss of reduction. These features are neither disclosed nor suggested by Everett et al. Indeed, there is no conversion of signals from an interlaced format to a non-interlaced format.

Moreover, such de-interlacing causes loss of quality in the displayed picture, which problem is overcome by embodiments of the claimed invention.

Because Everett et al. actively teaches away from the present invention and fails to teach or suggest important limitations of the claims, Applicant respectfully submits that the present invention is non-obvious over Everett et al.

In light of all of the above, it is submitted that the claims are in order for allowance, and prompt allowance is earnestly requested. Should any issues remain outstanding, the Examiner is invited to call the undersigned attorney of record so that the case may proceed expeditiously to allowance.

Respectfully submitted,



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